Notice : This is not a final specification. Some parametric limits are subject to change.

PM150CLA060

| Pre.	*T. Marumo*	Rev.	
Apr.	*M. Tahata 30-Aug '61*		

Feature
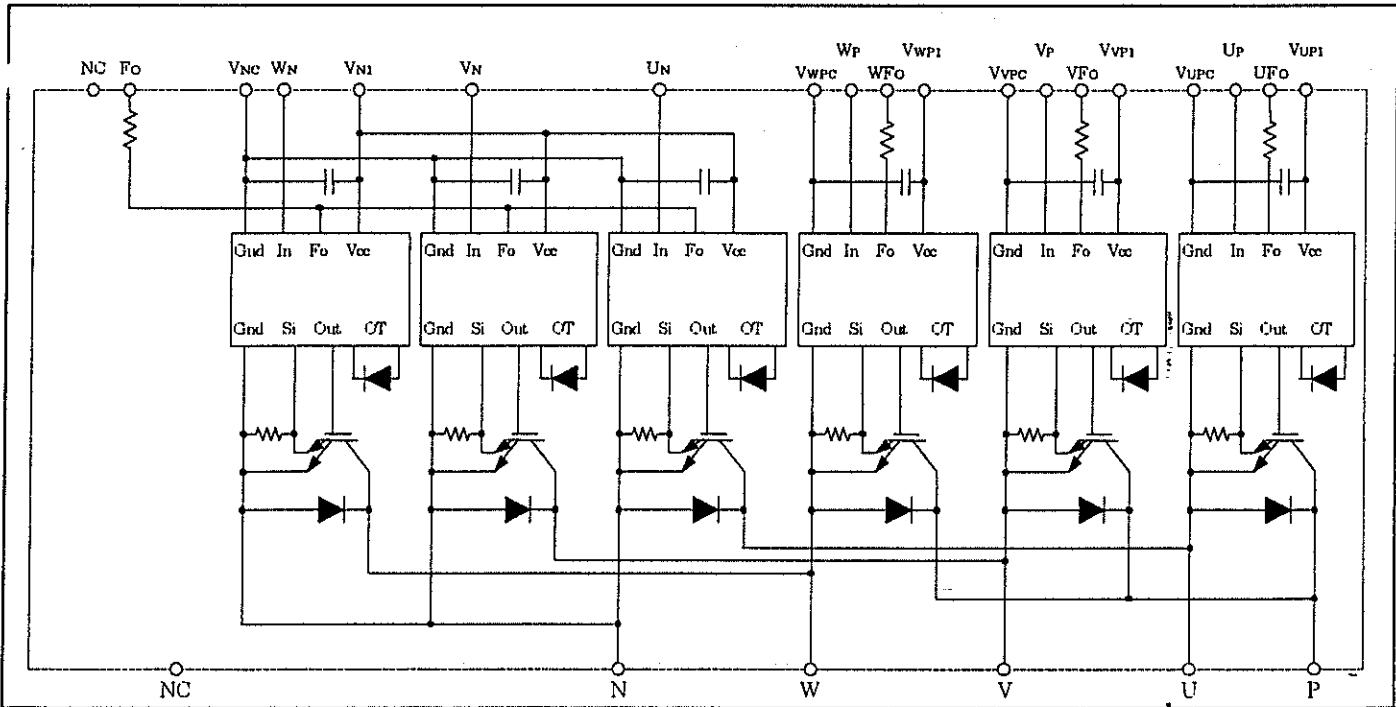
a) Adopting new 5th generation IGBT(CSTBT) chip, which performance is improved by 1μm fine rule process.

For example, typical Vce(sat)=1.5V @Tj=125°C

b) Adopt the over-temperature conservation by Tj detection of CSTBT chip, and error output is possiblefrom upper arm and a lower arm of IPM at all each protection.

c) New small package

Reduce the package size by 32%, thickness by 22% from S-DASH series.

· 3φ 150A, 600V Current-sense IGBT type inverter

· Monolithic gate drive & protection logic

· Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage (P-Fo available from upper arm devices)

· Acoustic noise-less 15kW/18.5kW class inverter application

OUTLINE DRAWING   Dimensions in mm

See Page 7

APPLICATION : General purpose inverter, servo drives and other motor controls

Maximum Ratings ($Tj = 25°C$, unless otherwise noted)

Inverter Part

Item	Symbol	Condition	Ratings	Unit
Collector-Emitter Voltage	V_{CES}	$V_D = 15V$, $V_{CIN} = 15V$	600	V
Collector Current	$\pm I_C$	$T_C = 25°C$	150	A
Collector Current (Peak)	$\pm I_{CP}$	$T_C = 25°C$	300	A
Collector Dissipation	P_C	$T_C = 25°C$	657	W
Junction Temperature	Tj		-20 ~ +150	°C

Control Part
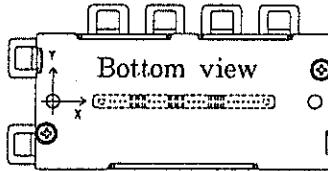
Item	Symbol	Condition	Rating	Unit
Supply Voltage	V_D	Applied between : V_{UP1}-V_{UPC} V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC}	20	V
Input Voltage	V_{CIN}	Applied between : U_P-V_{UPC}, V_P-V_{VPC} W_P-V_{WPC}, U_N-V_N-W_N-V_{NC}	20	V
Fault Output Supply Voltage	V_{FO}	Applied betwee : U_{FO}-V_{UPC}, V_{FO}-V_{VPC} W_{FO}-V_{WPC}, F_O-V_{NC}	20	V
Fault Output Current	I_{FO}	Sink current at U_{FO}, V_{FO}, W_{FO}, F_O terminals	20	mA

Total System

Item	Symbol	Condition	Rating	Unit
Supply Voltage Protected by SC	$V_{CC(PROT)}$	$V_D = 13.5～16.5V$ Inverter Part, Tj= +125°C Start	400	V
Supply Voltage (Surge)	$V_{CC(surge)}$	Applied between : P·N , Surge value	500	V
Module Case Operating Temperature	T_C	(Note-1)	-20 ~ +100	°C
Storage Temperature	Tstg		-40 ~ +125	°C
Isolation Voltage	Viso	60Hz, Sinusoidal Charged part to Base, AC 1 min.	2500	Vrms

(Note-1) Tc(under the chip) measurement point is below.   (unit : mm)

arm axis	UP		VP		WP		UN		VN		WN	
	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi	IGBT	FWDi
X	28.3	28.3	65.0	65.0	87.0	87.0	39.3	39.3	54.0	54.0	76.0	76.0
Y	-7.7	2.4	-7.7	2.4	-7.7	2.4	5.7	-4.4	5.7	-4.4	5.7	-4.4

Bottom view

Thermal Resistances

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Junction to case Thermal Resistances	$R_{th(j-c)Q}$	Inverter IGBT part (per 1/6) (Note-1)	—	—	0.19*	°C/W
	$R_{th(j-c)F}$	Inverter FWDi part (per 1/6) (Note-1)	—	—	0.32*	
Contact Thermal Resistance	$R_{th(c-f)}$	Case to fin, (per 1 module) Thermal grease applied	—	—	**	

* If you use this value, Rth(f-a) should be measured just under the chips.
** : This value is not specified yet.

Electrical Characteristics (Tj= 25°C unless otherwise noted)

Inverter Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Collector-Emitter Saturation Voltage	$V_{CE(sat)}$	$V_D=$ 15V, $V_{CIN}=$ 0V $I_C=$ 150A, Pulsed Fig.1	Tj= 25°C	–	1.5	2.0	V
			Tj=125°C	–	1.5	2.0	
FWDi Forward Voltage	V_{EC}	$-I_C=$ 150A, $V_{CIN}=$ 15V $V_D=$ 15V Fig.2		–	2.2	3.3	V
Switching Time	ton	$V_D=$ 15V, $V_{CIN}=$ 0V $\longleftrightarrow$ 15V		0.8	1.2	2.4	μs
	trr	$V_{CC}=$ 300V, $I_C=$ 150A		–	0.15	0.3	
	tc(on)	Tj= 125°C, Inductive Load		–	0.4	1.0	
	toff	Fig.3		–	2.0	2.8	
	tc(off)			–	0.6	1.2	
Collector-Emitter Cutoff Current	ICES	$V_{CE}=$ V_{CES} $V_D=$ 15V Fig.4	Tj= 25°C	–	–	1	mA
			Tj=125°C	–	–	10	

Control Part

Item	Symbol	Condition		Min.	Typ.	Max.	Unit
Circuit Current	I_D	$V_D=$ 15V	V_{N1}·V_{NC}	–	20	30	mA
		$V_{CIN}=$ 15V	V_{XP1}·V_{XPC}	–	6	10	
Input ON Threshold Voltage	$V_{th(ON)}$	Applied between : U_P-V_{UPC} , V_P-V_{VPC}		1.2	1.5	1.8	V
Input OFF Threshold Voltage	$V_{th(OFF)}$	W_P-V_{WPC} , U_N·V_N·W_N·V_{NC}		1.7	2.0	2.3	
Short Circuit Trip Level	SC	$-20 \leqq Tj \leqq 125$°C Fig.5,6 $V_D=$ 15V Fig.5,6		300	420	–	A
Short Circuit Current Delay Time	toff(SC)	$V_D=$ 15V Fig.5,6		–	10	–	μs
Over Temperature Protection	OT	Detect Tj of IGBT chip	Trip level	135	145	155	°C
	OTr		Reset level	–	125	–	
Supply Circuit Under-Voltage Protection	UV	$-20 \leqq Tj \leqq 125$°C	Trip level	11.5	12.0	12.5	V
	UVr		Reset level	–	12.5	–	
Fault Output Current	$I_{FO(H)}$	$V_D=$ 15V, $V_{CIN}=$ 15V		–	–	0.01	mA
	$I_{FO(L)}$		(Note-2)	–	10	15	
Minimum Fault Output Pulse Width	t_{FO}	$V_D=$ 15V	(Note-2)	1.0	1.8	–	ms

(Note-2) Fault output is given only when the internal SC, OT & UV protections schemes of either upper or lower arm device operate to protect it.

Mechanical Ratings and characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Mounting torque	—	Main terminal screw : M 5	2.5	3.0	3.5	N·m
Mounting torque	—	Mounting part screw : M 5	2.5	3.0	3.5	N·m
Weight	—	—	—	300	—	g

Recommended Conditions For Use

Item	Symbol	Condition	Recommended value	Unit
Supply Voltage	V_{CC}	Applied across P−N terminals	$\leqq 400$	V
Control Supply Voltage	V_D	Applied between : V_{UP1}-V_{UPC} V_{VP1}-V_{VPC}, V_{WP1}-V_{WPC}, V_{N1}-V_{NC} (Note-3)	15.0 ± 1.5	V
Input ON Voltage	$V_{CIN(ON)}$	Applied between : U_P-V_{UPC}, V_P-V_{VPC}	$\leqq 0.8$	V
Input OFF Voltage	$V_{CIN(OFF)}$	W_P-V_{WPC}, $U_N \cdot V_N \cdot W_N$-V_{NC}	$\geqq 4.0$	
PWM Input Frequency	f_{PWM}	Using Application Circuit of Fig.8	$\leqq 20$	kHz
Arm Shoot-through Blocking Time	t_{dead}	For IPM's each input signals Fig.7	$\geqq 2.0$	

(Note-3) With ripple satisfying the following conditions
dv/dt swing $\leqq \pm 5V/\mu s$, Variation $\leqq 2V$ peak to peak

Precautions for testing

1. Before appling any control supply voltage (V_D), the input terminals should be pulled up by resistores, etc. to their corresponding supply voltage and each input signal should be kept off state. After this, the specified ON and OFF level setting for each input signal should be done.

2. When performing "SC" tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
(These test should not be done by using a curve tracer or its equivalent.)
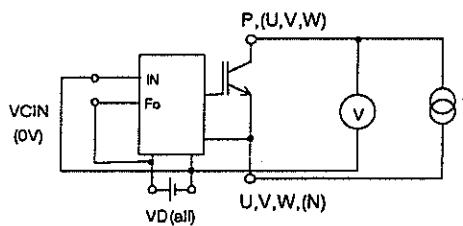
Fig.1 $V_{CE(sat)}$ Tset

Fig.2 V_{EC} Tset

a) Lower Arm Switching
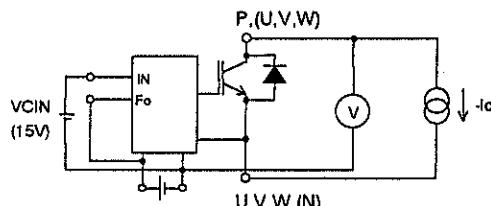
b) Upper Arm Switching
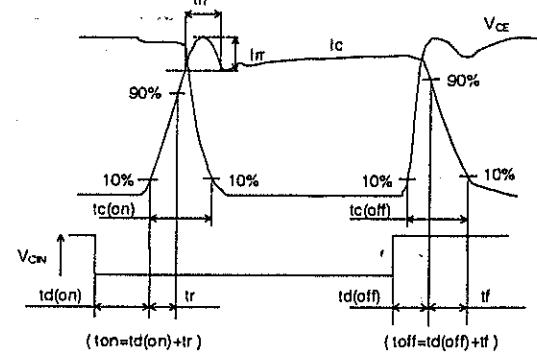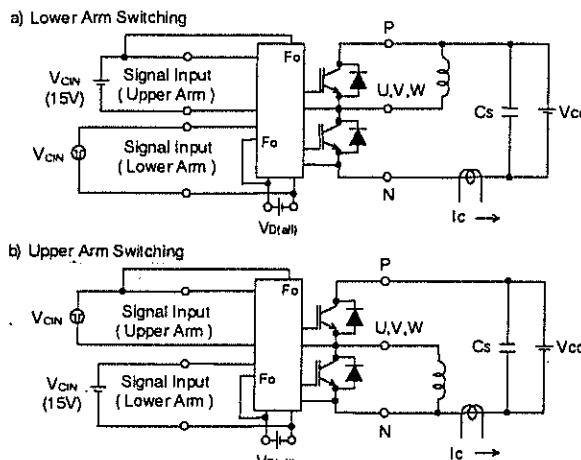
Fig.3 Switching time test circuit and waveform
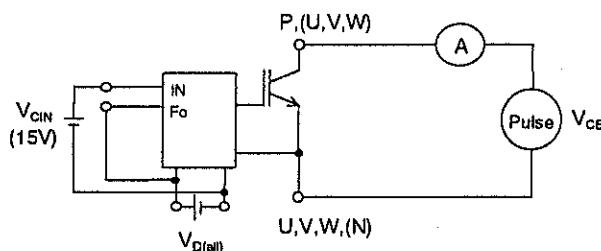
Fig4 ICES Test
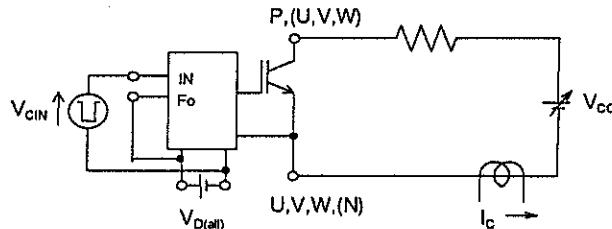
Fig.5 SC Test
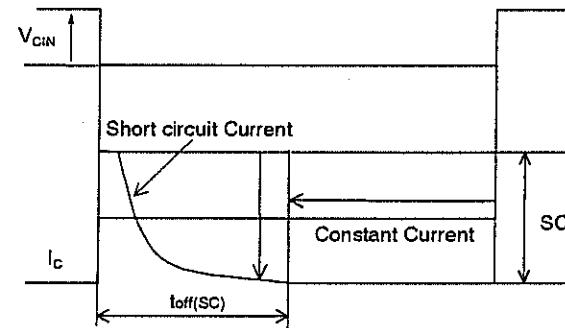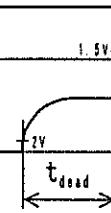
Fig.6 SC Test waveform

IPM' input signal V_{CIN} (Upper Arm)

IPM' input signal V_{CIN} (Lower Arm)
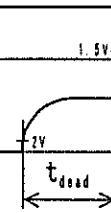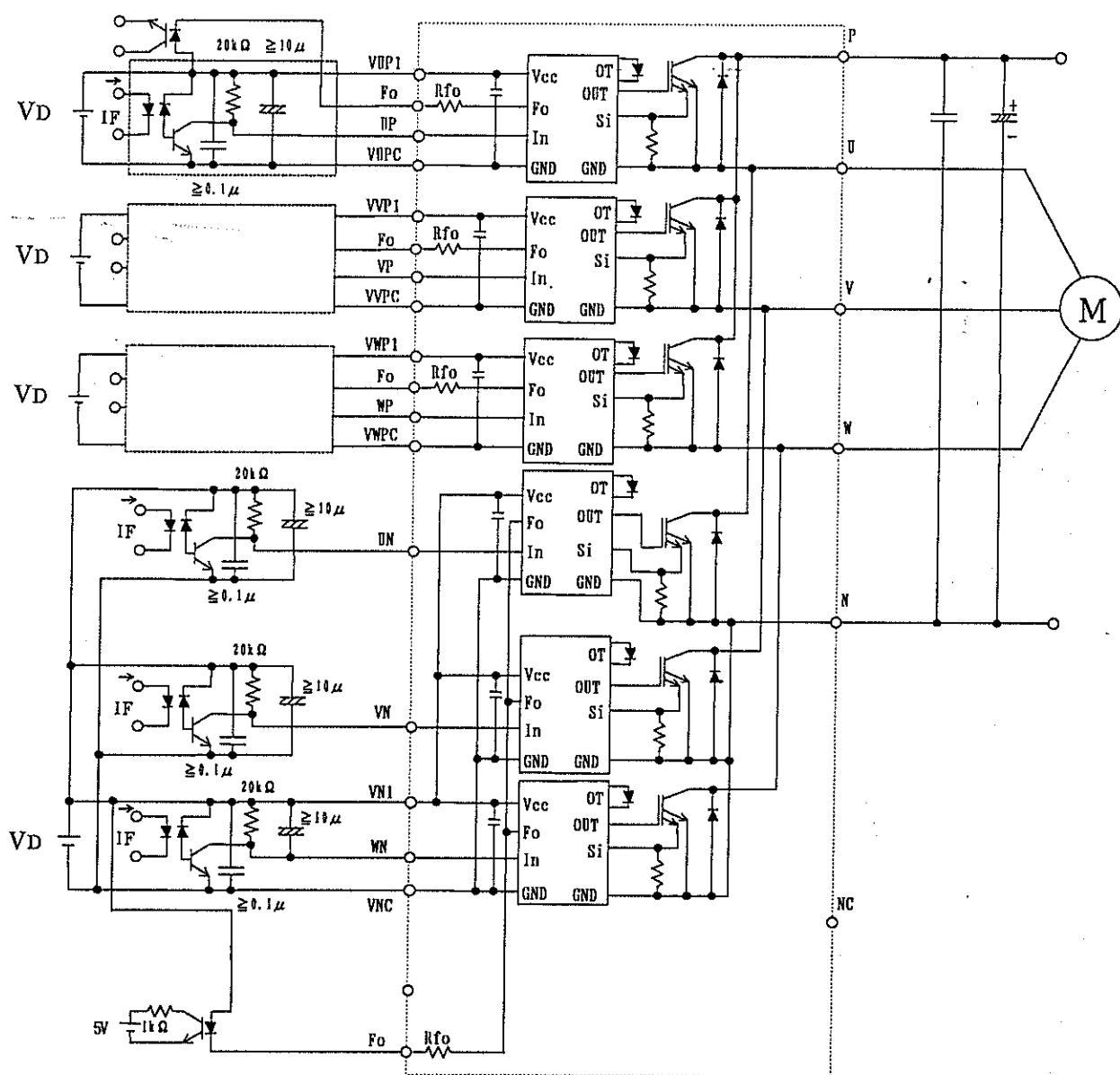
1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

Fig.7 Dead time measurement point example

[ ] : Interface which is the same as the U-phase
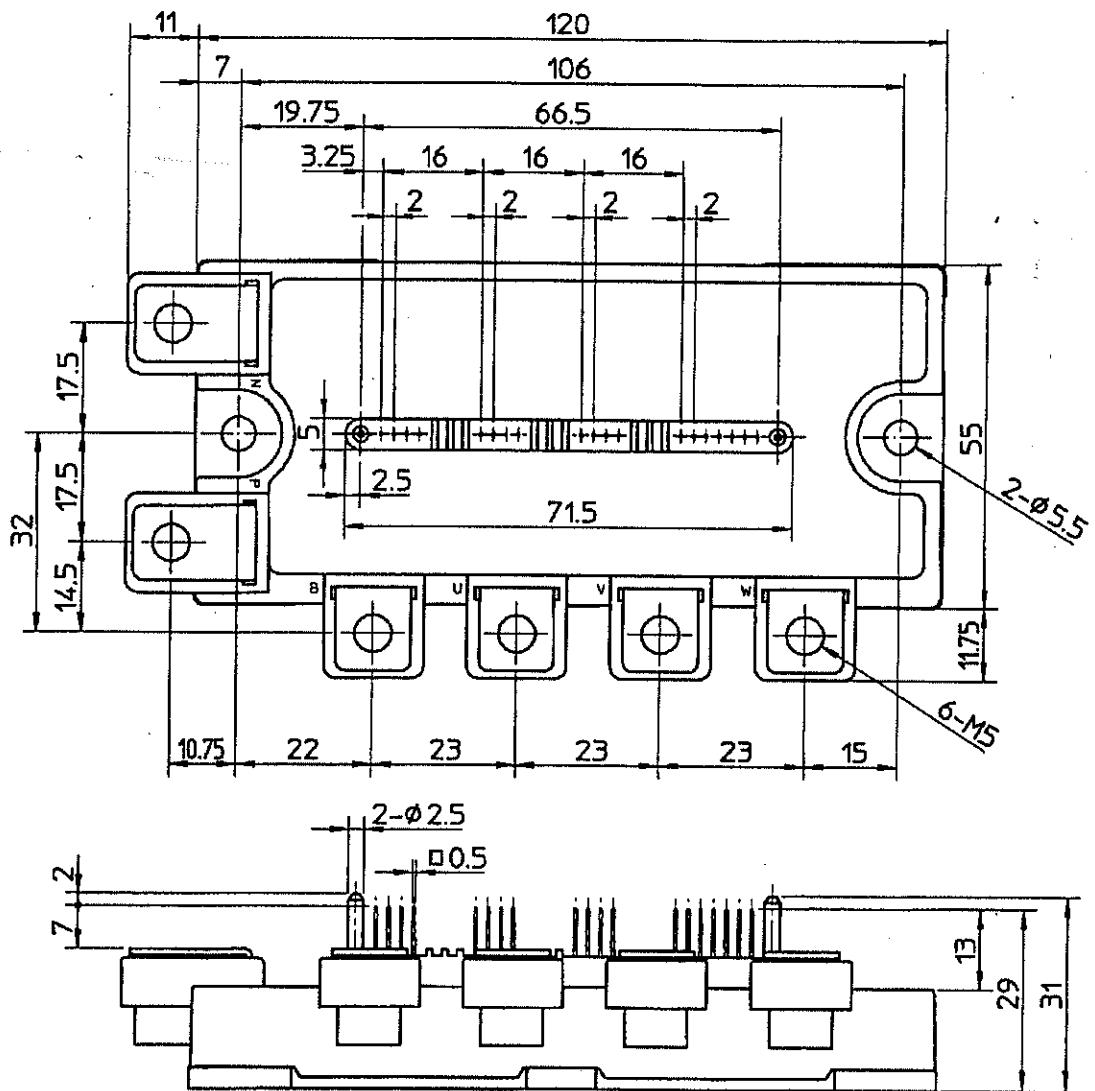
## Fig. 8 Application Example Circuit

Notes for stable and safe operation ;

● Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.

● Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.

● Fast switching opto-couplers : tPLH, tPHL ≦ 0.8 μs, Use High CMR type.

● Slow switching opto-coupler : CTR > 100%

● Use 4 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.

● Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between P and N terminal.

● Use line noise filter capacitor (ex. 4.7nF) between each input AC line and ground to reject common -mode noise from AC line and improve noise immunity of the system.

Outline drawings

[Dimensions in mm]

Terminal code

1. VUPC	6. VFO	11. WP	16. UN
2. UFO	7. VP	12. VWP1	17. VN
3. UP	8. VVP1	13. VNC	18. WN
4. VUP1	9. VWPC	14. VN1	19. Fo
5. VVPC	10. WFO	15. NC	